tion, illustrating how the trigger voltage Vt1 may be adjusted by changing values of R and/or by electrically cascading or stacking modular ESD stages.

DETAILED DESCRIPTION OF THE INVENTION

[0017] The following detailed description is merely exemplary in nature and is not intended to limit the invention or the application and uses of the invention. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, or the following detailed description.

[0018] For simplicity and clarity of illustration, the drawing figures illustrate the general manner of construction, and descriptions and details of well-known features and techniques may be omitted to avoid unnecessarily obscuring the invention. Additionally, elements in the drawings figures are not necessarily drawn to scale. For example, the dimensions of some of the elements or regions in the figures may be exaggerated relative to other elements or regions to help improve understanding of embodiments of the invention.

[0019] The terms "first," "second," "third," "fourth" and the like in the description and the claims, if any, may be used for distinguishing between similar elements and not necessarily for describing a particular sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments of the invention described herein are, for example, capable of operation in sequences other than those illustrated or otherwise described herein. Furthermore, the terms "comprise," "include," "have" and any variations thereof, are intended to cover non-exclusive inclusions, such that a process, method, article, or apparatus that comprises a list of elements is not necessarily limited to those elements, but may include other elements not expressly listed or inherent to such process, method, article, or apparatus. The term "coupled," as used herein, is defined as directly or indirectly connected in an electrical or non-electrical manner.

[0020] While the circuits of FIGS. **2** and **3** can be effective in providing ESD protection, further improvements are desirable. Accordingly, there is an ongoing need to provide improved ESD clamps, especially ESD clamps that are adapted to achieve a variety of predetermined trigger voltages, and that are bidirectional so as to conserve chip area, and that are modular in nature so as to electrically stackable, and that are less sensitive to manufacturing variations that can adversely affect manufacturing yield. Other desirable features and characteristics of the present invention will become apparent from the subsequent detailed description of the invention and the appended claims, taken in conjunction with the accompanying drawings and this background of the invention.

[0021] FIG. **5** is a simplified schematic diagram illustrating internal components of ESD clamp **41**, according to an embodiment of the present invention. ESD clamp **41** is used in generalized protection circuit **10** in place of ESD clamp **11**. ESD clamp **41** differs from prior art ESD clamps **21**, **31** of FIGS. **2** and **3** in that it utilizes two mirror coupled transistor stages T**1** and T**2** joined at node **52** and further does not have Zener diode **13**. Transistor stage T**1** comprises transistor **25** analogous to transistor **25** of FIGS. **2-3** with emitter **26**, collector **27** and base **28**, plus resistor **29**, coupled in generally the same manner as in FIGS. **2** and **3**. The same reference numbers are used for transistor stage T**1** and ESD clamp **31** of FIG. **3**, to indicate that the individual elements are analogous but not necessarily identical. Resistor **29** is coupled between base **28** at node **34** and emitter **26** at node **32**. Node **32** is adapted to be coupled to GND terminal **23** of ESD protection circuit **10** of FIG. **1**. Transistor stage T**2** comprises transistor **35** having emitter **36**, collector **37** and base **38**. Resistor **39** is coupled between base **38** at node **44** and emitter **36** at node **42**. Node **43** of Transistor stage T**2** is coupled to node **33** of transistor stage T**1** via node **52**. Nodes **33**, **52** and **43** are shown as separate nodes merely for convenience of description and can be combined. Node **42** of Transistor stage T**2** is adapted to be coupled to input/output (I/O) terminals **22** of ESD circuit **10** of FIG. **1**. It will be noted that while stages T**1** and T**2** of ESD clamp **41** individually resemble ESD clamp **31** of FIG. **3**, they are serially coupled in opposition or in mirror arrangement, that is, node **43** of transistor stage T**2** is coupled to node **33** of transistor stage T**1**, or to say it another way, collector **27** of transistor stage T**1** is coupled to collector **37** of transistor stage T**2** via common node **52**. An advantage of ESD clamp **41** compared to ESD clamps **21** and **31** is that ESD clamp **41** is bi-directional, that is, it will respond, for example, to a positive going ESD transient at either of terminals **22** or **23** of ESD circuit **10**. This is a significant advantage since it results in a substantial area saving in providing bi-directional ESD protection to circuit core **24**, and thereby lowers the cost of manufacture of the SC device or IC containing circuit core **24** of FIG. **1**.

[0022] FIGS. **6-7** are simplified schematic diagrams illustrating internal components of ESD clamps **51**, **61** according to further embodiments of the present invention, wherein it will be understood that clamps **51**, **61** are substituted for clamp **11** in generalized ESD protection circuit **10** of FIG. **1**. ESD clamp **51** differs from ESD clamp **41** of FIG. **5** in that it comprises two serially coupled ESD stages, that is, lower ESD stage or clamp **41** (e.g., clamp **41** of FIG. **5**) and upper ESD stage or clamp **41'** (also analogous to clamp **41** of FIG. **5**). ESD clamp **61** differs from ESD clamp **51** of FIG. **6** in that it comprises three serially coupled ESD stages, that is, lower ESD stage or clamp **41**, intermediate ESD stage or clamp **41'** and upper or end ESD stage or clamp **41"**. The terms "lower" or "first" and "upper" or "end" or "last" are used herein merely to indicate that one of the serially coupled ESD stages (e.g., "lower or "first" ESD clamp **41**) is coupled to so-called GND terminal **23** of ESD circuit **10** and another of the serially coupled ESD stages (e.g., "upper" or "end" or "last" clamp **41'** or **41"**) is coupled to so-called I/O terminals **22** of ESD circuit **10** of FIG. **1**, wherein GND is usually (but not always) the lower potential side of circuit **10** and the I/O terminals are coupled to what is usually (but not always) the higher potential side of ESD circuit **10**. The designations of "lower" or "first" and "upper" or "end" or "last" are merely for convenience of reference and not intended to be limiting. Lower ESD stage or clamp **41** is described in connection with FIG. **5**. Intermediate and upper ESD stages or clamps **41'** and **41"** are analogous to lower ESD stage or clamp **41** and the convention is adopted of identifying the individual components thereof analogous to those of lower ESD stage or clamp **41** by adding a prime to the individual reference numbers of intermediate stage or clamp **41'** and a double prime to the individual reference numbers of upper or end or last stage or clamp **41"**, for example, emitters **26'**, **26"** of intermediate and upper ESD stages or clamps **41'**, **41"** are analogous to emitter **26** of lower ESD stage or clamp **41**, collectors **27'**, **27"** to collector **27**, and so forth. ESD stages or clamps **41**, **41'**, **41"** are coupled so that: (i) node **42** of lower or first stage or clamp